Refine Search

Search Results -

Terms	Documents
L48 or L47	84

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L49

[Refine Search]

[Recall Text] [Clear] [Interrupt]

Search History

DATE: Monday, November 29, 2004   Printable Copy   Create Case

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ

Set Name side by side	Query	Hit Count	Set Name result set
L49	L48 or l47	84	L49
L48	l27 or l26	39	L48
L47	L46 or l45	60	L47
L46	l33 or l34 or l35	37	L46
L45	L44 or l43 or l42 or l41	23	L45
L44	l37 and l18	22	L44
L43	l37 and l17	1	L43
L42	L40 and l18	17	L42
L41	L40 and l17	1	L41
L40	L37 and dma	36	L40
L39	L37 and dam	0	L39
L38	L37 and l31	0	L38
L37	(debug$5 near3 message$1) and (channel near2 transfer$1)	42	L37

h   e b   b cg b   e e ch

L36	(debug$5 near3 message$1) same (channel near2 transfer$1)	0	L36
L35	L31 and (transfer$5 near3 error$1)	23	L35
L34	L32 and (debug$5 near3 message$1)	9	L34
L33	L32 and message$1	27	L33
L32	L31 and debug$5	30	L32
L31	dma same (communication bus$4)	208	L31
L30	L28 and (debug$5 port$1)	0	L30
L29	L28 and (debug$5 message$1)	0	L29
L28	(system unit$1) same (communication$1 bus$5)	22	L28
L27	(debug$5 near2 (module$1 or device$1)) same (debug$5 message$1)	12	L27
L26	l5 or l7 or l8 or L24	27	L26
L25	l5 or 7 or l8 or L24	9588600	L25
L24	L22 or l21 or l20	23	L24
L23	l6 and l17	0	L23
L22	l6 and l18	15	L22
L21	l9 and l18	23	L21
L20	l11 and l18	22	L20
L19	l11 and l17	0	L19
L18	709/$.ccls.	32424	L18
L17	714/$.ccls.	47130	L17
L16	(debug message$1) and (DMA channel transfer$1)	0	L16
L15	(debug message$1) and (dma channel transfer$1)	0	L15
L14	(debug message$1) and (dma channel transfer boundary)	0	L14
L13	(debug message$1) same (dma channel transfer boundary)	0	L13
L12	(identif$5 near3 debug message$1) same (dma channel transfer boundary)	0	L12
L11	l4 and l2	56	L11
L10	l1 and l2	8345	L10
L9	l1 and l4	66	L9
L8	(debug control circuit$4) and ((direct memory access$5) or dma)	3	L8
L7	(debug control circuit$4) same ((direct memory access$5) or dma)	1	L7
L6	L4 and (((direct memory access$5) or dma) near3 channel$1)	35	L6
L5	L4 same (((direct memory access$5) or dma) near3 channel$1)	1	L5
L4	debug$5 near3 message$1	687	L4
L3	debug$5 same l1	271	L3
L2	channel$1 and l1	8345	L2
L1	((direct memory access$5) or dma) same bus$5	18474	L1

END OF SEARCH HISTORY

h   e   b   b   cg b   e   e   ch